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Performance Analysis of High Speed DDR3 SDRAM Controller

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Abstract: As the system bandwidth continues to increase, memory technologies have been privileged for high speed operation and performance.DDR3 SDRAM is the third generation of DDR memories rapidly developing with high density high memory bandwidth and low device cost. However, because of high speed interface technology and complex instruction based memory a special purpose memory controller is necessary for optimizing the burst access to increase data throughput. In this paper, a specific purpose DDR3 controller for high performance table look up is proposed and a corresponding lookup circuit based on the Hash Cam approach is presented.

Key words: DDR3, SDRAM, VERILOG.

I.INTRODUCTION

Synchronous dynamic random access memory(SDRAM) is synchronized with system bus, for asynchronous interface the DRAM responds as early as possible to changes in control inputs and the SDRAM has a synchronous interface ,it waits a clock signal before responding to control inputs.DDR3 SDRAM transfers the data at twice the rate of DDR2 SDRAM which enables higher bandwidth while DDR2 uses 4n-prefetch and DDR3 uses 8n-prefetch[1]. A 64-bit DDR3 SDRAM may achieve a transfer rate up to 64 times the memory clock speed in megabytes per second(MB/s).In addition , the DDR3 standard permits the chip capacities of up to 8 gigabits .Content Addressable Memory (CAM) based techniques are widely used in network equipment for fast table look up[2]. When it comes to RAM technology and CAM technology, CAM technology is confined in few aspects like hardware cost, memory density and power dissipation. Recently a HASH-CAM circuit [3], which Combines the merits of hash algorithm and the CAM function, was proposed to replace pure CAM based Look up circuits with comparable performance, higher memory density and lower cost. Efficient DDR bandwidth [4] utilization is the major challenge for lookup functions that exhibit short and random memory access patterns. The off-chip low cost, high density DDR memory technology has now become an attractive alternative for proposed HASH-CAM based lookup circuit. However DDR technology optimized for burst access. This paper presents DDR3 SDRAM controller architecture to achieve high speed operation by using Xilinx FPGA technology.

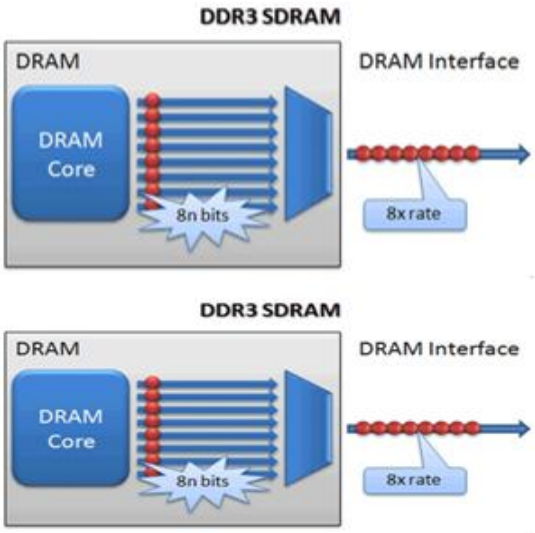

Fig1: Generations of DRAMs and their Data rates

II.RELATED WORK

DDR memory's primary advantage is the ability to fetch the data on both rising falling edge of a clock Cycle, doubling the data rate for a clock cycle.

Memory temporization is given through a series of numbers, such as 2-3-2-6-T1,3-4-4-8 or 2-2-2-5for DDR1.These numbers indicate the number of clock

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pulses that it takes the memory to perform a certain operation-the smaller the number faster the operation.
The operations that these numbers represent the CL-tRCD-tRP-tRS-CMD[5].

CL: Column address Strobe (CAS) latency is the time it takes between the processor asking memory for data and memory returning it.
tRCD: ROW Address Strobe (RAS) to CAS delay is the time it takes between the activation of the row (RAS) and the column (CAS) where data is stored in the matrix.
tRP: RAS precharge is the time between disabling the access to a row of data and the beginning of the access to another row of data.
tRAS: Active to precharge delay is how long the memory has to wait until the next access to memory can be initiated.
CMD: Command rate is the time between the memory chip activation and when the initial starting command may be sent to the memory. But this value may not be informed. Because of the burst write/read mode and the multi bank architecture, simultaneous operations on different banks are allowed in SDRAMs. We can achieve high memory bandwidth by scheduling the memory access to each and every bank.

Many SDRAMs focus on bank control and data access sequences to achieve a better system performance. To improve memory bandwidth [6] and power consumption in video applications, new memory-interface architecture is proposed. An address-translation technique can be adopted as architecture in order to utilize the fact that video processing algorithms have memory-access patterns which are regular. We can minimize the number of overhead cycles by translation which are needed for row-activations in synchronous DRAM (SDRAM).
The architecture of the present video processing[7] units in consumer systems is usually based on various forms of processor .The present video processing unit architecture in consumer system is usually based on various types of processor hardware making communication with an off-chip SDRAM memory. The general examples are MPEG encoders and decoders and high end television systems. Based on the dual-core platform, the memory management system for multimedia application is performed. In order to reduce the memory bus transition and have efficient bus bandwidth, 2 steps store optimization in control level has been adopted and nearly 35% bus efficiency increase is observed when compared with before scheme. To compliment different master requirements, a reasonable schedule level arranges memory access priority.

III.DESIGN METHODOLOGY

DDR3 SDRAM devices are the next generation devices in the DDR SDRAM family. These devices use 1.5V signaling.DDR3 SDRAM devices use DDR architecture to achieve high speed operation .The memory operates using a differential clock provided by the controller.DDR3 memory is more flexible to be accessed with fewer bank conflicts. The proposed Hash-CAM based lookup circuit is shown in fig 2.

Fig2:Hash-CAM lookup circuit using DDR3 SDRAMs

The original data and reference address information are stored in DDR3 SDRAM.A data is given to the Hash-CAM circuit where an address is generated. The translation of instructions and addresses is done when the address value is sent from DDR3 SDRAM interface which is later recognized by DD3 memory. The stored data &addresses in the memory are read back to the Hash-CAM circuit in order to validate the match.

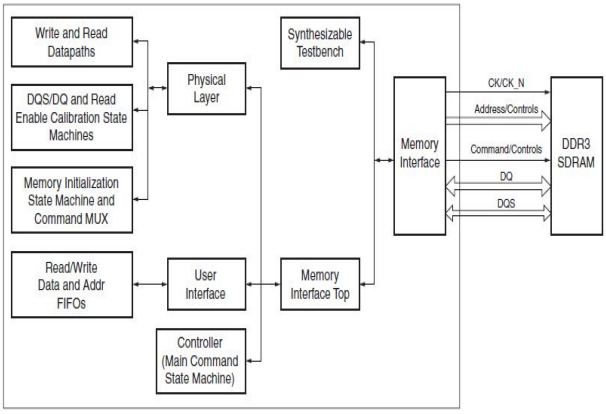

Fig 3:DDR3 SDRAM interface

As a part of DDR3 reference design. The address and the data patterns are provided by backend to test write and read accesses between memory device and memory interface.

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A bidirectional data strobe (DQS) [8] is transmitted along with the data for use in data capture at the receiver.DQS is strobe transmitted by the DDR3 SDRAM device during Reads and by the controller while writing DQS when it is center aligned with data for Writes and edge aligned data for Reads.

IV.DDR3 SDRAM COMMANDS

Commands are registered at every positive edge of the clock. Read and Write accesses to the DDR3 SDRAM device are burst oriented .Accesses begin with the registration of an active command, which is then followed by Read or Write command.

Precharge Command

The precharge command is used to deactivate the open row in a particular bank. The bank is available for subsequent row activation for a specified time after the precharge command is issued.

Auto Refresh Command

For every 7.8 µs the DDR3 device must be refreshed. Within the controller, the circuit to flag the Auto Refresh Command is built. With the help of system clock, the controller which is divided by 16, to make the counter refresh.

Active Command

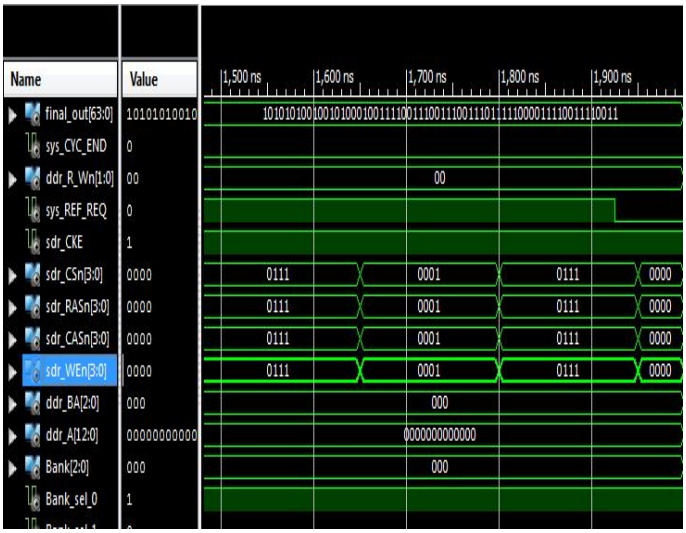
Within a back, the DDR3 SDRAM memory issues Read or Write commands, and then by using a Active Command a row in the bank is activated, Later a row is opened, read or write commands to the row are issued.

Read Command

The Read command is used to initiate a burst read access to an active row. After the read burst is over, the row is still available for subsequent access until it is precharge.

V.EXPERIMENTAL RESULTS AND ANALYSIS

In this paper a high speed DDR3 SDRAM controller has been designed with 64-bit data transfer which synchronizes the transfer of data between DDR RAM and external peripheral devices like host computer and laptop and so on. The simulation results for top module are shown in figure4.



. Fig 4: DDR3 SDRAM Top Module simulation results

The complete lookup circuit was simulated using Xilinx technology .The off-chip power dissipation in this work is 39mW.Reduced power consumption due to 90nm fabrication technology. Prefetch buffer is doubled to 8 bits to further increase performance.

Table 1.Performance of DDR3 Hash-CAM lookup circuit

Hash-CAM data width	64 bits
Hash-CAM table entrants	256K
CAM-RAM depth	512
Hash Function	CRC-16
Lookup Frequency	216MHz
Combinational/Memory ALUTs	292
Registers	20747

The above experimental results clearly validate the expected performance of the proposed DDR3 SDRAM controller architecture. For a given random look up the DDR3 peak memory bandwidth can be achieved.

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VI.CONCLUSION

In this paper, an advanced DDR3 memory controller architecture for high performance table lookup is proposed. The proposed DDR3 Hash-CAM circuit is prototyped for a 256K table entry. The advantages of DDR3 SDRAM controller compared to SDR SDRAM, DDR1 SDRAM, DDR2 SDRAM is that it synchronizes the data transfer, and the data transfer is twice as fast as previous, the production cost is also very low. Hence DDR3 SDRAM controller successfully designed using verilog HDL and simulated using Model Sim.

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